WHAT IS CLAIMED IS:

1. A frequency synthesizing circuit, the circuit being digital, comprising:

a multiplexor having at least a first input, a second input, an output, and a control terminal;

a controller having at least an input and an output, wherein the output coupling to the control terminal of the multiplexor provides at least one-bit signal to select either data feeding the first input or data feeding the second input of the multiplexor to pass the multiplexor;

a first memory device coupling to the first input of the multiplexor for storing a first reference frequency;

a second memory device coupling to the second input of the multiplexor for storing a second reference frequency;

a linear feedback shift register coupling to the input of the controller, wherein the linear feedback shift register stores a target frequency so as to compare with a predeter- mined threshold in sequence; and

a digital clock signal for clocking a sequential operation of the frequency synthe- sizing circuit.

2. The sequential operation of the frequency synthesizing circuit as recited in claim 1, wherein

the target frequency is compared with the predetermined threshold for determining either data feeding the first input of the multiplexor or data feeding the second input of the multiplexor to pass to the output of the multiplexor depending on the target frequen- cy being larger or smaller than the predetermined threshold, and

the target frequency is shifted by one position for next comparison until a minimal resolution does not distinguish a difference between the target frequency and the predetermined threshold.

3. The first reference frequency and the second reference frequency stored in the first memory device and the second memory device respectively as recited in claim 1, wherein the reference frequencies are sampled from sinusoidal waves.

4. The linear feedback shift register of the frequency synthesizing circuit as recited in claim 1, wherein an order of the linear feedback shift register determines the minimal resolution.

5. The minimal resolution of the frequency synthesizing circuit as recited in claim 2, wherein the minimal resolution is determined by a ratio of a difference between the first reference frequency and the second reference frequency to a two's power, the power is the order of the linear feedback shift register.

6. A frequency synthesizing system, comprising:

a multiplexor having at least a first input, a second input in parallel, an output, and a control terminal;

a controller having at least an input and an output, wherein the output coupling to the control terminal of the multiplexor provides at least one-bit signal to select either data feeding the first input or data feeding the second input of the multiplexor to pass;

a first memory device coupling to the first input of the multiplexor for storing transformation of a first reference frequency;

a second memory device coupling to the second input of the multiplexor for storing transformation of a second reference frequency;

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a linear feedback shift register coupling to the input of the controller, wherein the linear feedback shift register stores a target frequency so as to compare with a predetermined threshold in sequence; and

a digital clock signal for clocking a sequential operation of the frequency synthesizing system.

7. The sequential operation of the frequency synthesizing system as recited in claim 6, wherein

the target frequency compared with the predetermined threshold for determining either data feeding the first input of the multiplexor or the second input of the multiplexor to pass to the output of the multiplexor depending on the target frequency being larger or smaller than the predetermined threshold, and

the target frequency is shifted by one position for next comparison until a minimal resolution does not distinguish a difference between the target frequency and the predetermined threshold.

8. The transformation of the first reference frequency and the second reference frequency stored in the first memory device and the second memory device respectively as recited in claim 6, wherein the transformation is sinusoidal function.

9. The linear feedback shift register of the frequency synthesizing system as recited in claim 6, wherein an order of the linear feedback shift register determines an order of the minimal resolution.

10. The minimal resolution of the frequency synthesizing system as recited in claim 7, wherein the minimal resolution is determined by a ratio of a difference between the

first reference frequency and the second reference frequency to two to the power of the order of the linear feedback shift register.